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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,344	01/10/2002	Jae Soo Park	1016-012	8012

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,344	PARK ET AL	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Serial Number: 10/044344 Attorney's Docket #: 1016-012
Filing Date: 1/10/2002;

Applicant: Park et al.

Examiner: Alexander Williams

Applicant's Amendment in Paper # 3, filed 6/29/03 has been acknowledged.

Applicant is reminded of the proper content of an abstract of the disclosure **(For example, this is a device patent application, not a method application. The term "method" should be replaced with "device" in the first line of the abstract).**

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Lee et al. (U.S. Patent # 6,130,074).

1. Lee et al. (figures 1 to 22) specifically figures 9 and **10 (see figure 10 for a clear understanding of the vias 950 and the dielectric material 945l in the dielectric layer)** show an integrated circuit interconnect **comprising**: a wide top metal line **960**; a wide bottom metal line **940**; a dielectric layer **945l** disposed between the wide top and

wide bottom metal lines; a plurality of vias **950** in the dielectric layer and connecting the wide top and wide bottom metal lines **including**: a first via **(for example, first row and first via)** having a width, and a second via **(for example, first row and fourth via, therefore leaving two vias between the first and the fourth via)** having a width and spaced more than two widths away and less than four widths away from the first via **(see column 5, line 1 to column 6, line 39)**.

2. The integrated circuit as claimed in claim 1 wherein: Lee et al.'s second via is spaced from the first via in a direction perpendicular to the length of the wide top metal line; and including: a third via having a width and spaced more than two widths and less than four widths from the first via in a direction parallel to the length of the wide top metal line.

3. The integrated circuit as claimed in claim 1 wherein: Lee et al.'s second via is spaced from the first via in a direction parallel to the length of the wide top metal line; and including: a third via having a width and spaced more than two widths and less than four widths from the first via in a direction perpendicular to the wide top metal line.

4. The integrated circuit as claimed in claim 1 wherein: Lee et al.'s dielectric layer has an opening provided therein equidistant from the first and second vias.

5. The integrated circuit as claimed in claim 4 wherein: Lee et al.'s opening which has a width equal to the width of the first via.

6. The integrated circuit as claimed in claim 4 wherein: Lee et al.'s opening has a length greater than twice the width thereof.

7. The integrated circuit as claimed in claim 4 wherein: Lee et al.'s opening has a length and the length extends perpendicular to the length of the wide top metal line.

8. Lee et al. (figures 1 to 22) specifically figures 9 and **10 (see figure 10 for a clear understanding of the vias 950 and the dielectric material 945l in the dielectric layer)** show an integrated circuit interconnect **comprising**: a wide top metal line **960**; a wide bottom metal line **940**; a dielectric layer **945l** disposed between the wide top and wide bottom metal lines; and a via-sea **950** in the dielectric layer and connecting the wide top and wide bottom metal lines **including**: a first column of vias **(for example, first row of vias)**, having a width, and a second column of vias **(fourth row of vias)** having a width and spaced more than two widths away and less than four widths away from the first column of vias **(see column 5, line 1 to column 6, line 39)**.

9. The integrated circuit as claimed in claim 8 wherein: Lee et al.'s second column of vias is spaced from the first column of vias in a direction perpendicular to the length of the wide top metal line; and including: a first row of vias including a via in the first

column of vias having a width and spaced more than two widths and less than four widths from the first column of vias in a direction parallel to the wide top metal line.
10. The integrated circuit: as claimed in claim 8 wherein: Lee et al.'s second column of vias is spaced from the first column of vias in a direction parallel to the length of the wide top metal line; and including: a first row of vias including a via in the first column of vias having a width and spaced more than two widths and less than four widths from the first column of vias in a direction perpendicular to the wide top metal line.
11. The integrated circuit as claimed in claim 8 wherein: Lee et al.'s dielectric layer has an opening provided therein equidistant from the first column of vias and the second column of vias.
12. The integrated circuit as claimed in claim 11 wherein: Lee et al.'s opening has a width equal to the width of the first column of vias.
13. The integrated circuit as claimed in claim 11 wherein: Lee et al.'s opening has a length greater than twice the width thereof.
14. The integrated circuit as claimed in claim 11 wherein: Lee et al.'s opening has a length and extends perpendicular to the length of the wide top metal line.

Claims 1 to 14 are rejected under 35 U.S.C. § 102(e) as being anticipated by Chittipeddi et al. (U.S. Patent # 6,417,087 B1).
1. Chittipeddi et al. (figures 1 to 4M) specifically figures 2 and 3 show an integrated circuit interconnect **40 comprising**: a wide top metal line **17**; a wide bottom metal line **5**; a dielectric layer **11** disposed between the wide top and wide bottom metal lines; a plurality of vias **19** in the dielectric layer and connecting the wide top and wide bottom metal lines **including**: a first via **(for example, first row first via)** having a width, and a second via **(for example, third row first via)** having a width and spaced more than two widths away and less than four widths away from the first via.
2. The integrated circuit as claimed in claim 1 wherein: Chittipeddi et al.'s second via is spaced from the first via in a direction perpendicular to the length of the wide top metal line; and including: a third via having a width and spaced more than two widths and less than four widths from the first via in a direction parallel to the length of the wide top metal line.
3. The integrated circuit as claimed in claim 1 wherein: Chittipeddi et al.'s second via is spaced from the first via in a direction parallel to the length of the wide top metal line;

and including: a third via having a width and spaced more than two widths and less than four widths from the first via in a direction perpendicular to the wide top metal line.

4. The integrated circuit as claimed in claim 1 wherein: Chittipeddi et al.'s dielectric layer has an opening provided therein equidistant from the first and second vias.

5. The integrated circuit as claimed in claim 4 wherein: Chittipeddi et al.'s opening which has a width equal to the width of the first via.

6. The integrated circuit as claimed in claim 4 wherein: Chittipeddi et al.'s opening has a length greater than twice the width thereof.

7. The integrated circuit as claimed in claim 4 wherein: Chittipeddi et al.'s opening has a length and the length extends perpendicular to the length of the wide top metal line.

8. Chittipeddi et al. (figures 1 to 4M) specifically figures 2 and 3 show an integrated circuit interconnect comprising: a wide top metal line **17**; a wide bottom metal line **5**; a dielectric layer **11** disposed between the wide top and wide bottom metal lines; and a via-sea **19** in the dielectric layer and connecting the wide top and wide bottom metal lines including: a first column of vias **(for example, first row)**, having a width, and a second column of vias **(for example, third row)** having a width and spaced more than two widths away and less than four widths away from the first column of vias.

9. The integrated circuit as claimed in claim 8 wherein: Chittipeddi et al.'s second column of vias is spaced from the first column of vias in a direction perpendicular to the length of the wide top metal line; and including: a first row of vias including a via in the first column of vias having a width and spaced more than two widths and less than four widths from the first column of vias in a direction parallel to the wide top metal line.

10. The integrated circuit: as claimed in claim 8 wherein: Chittipeddi et al.'s second column of vias is spaced from the first column of vias in a direction parallel to the length of the wide top metal line; and including: a first row of vias including a via in the first column of vias having a width and spaced more than two widths and less than four widths from the first column of vias in a direction perpendicular to the wide top metal line.

11. The integrated circuit as claimed in claim 8 wherein: Chittipeddi et al.'s dielectric layer has an opening provided therein equidistant from the first column of vias and the second column of vias.

12. The integrated circuit as claimed in claim 11 wherein: Chittipeddi et al.'s opening has a width equal to the width of the first column of vias.

13. The integrated circuit as claimed in claim 11 wherein: Chittipeddi et al.'s opening has a length greater than twice the width thereof.
14. The integrated circuit as claimed in claim 11 wherein: Chittipeddi et al.'s opening has a length and extends perpendicular to the length of the wide top metal line.

Response

Applicant's arguments filed 6/29/03 have been fully considered, but are not found to be persuasive in view of the modified grounds of rejections detailed above. Appllicant's arguments on pages 6 to 9 have been ackowledged but are not found to be persuasive in view of the modified rejection detailed above. Applicant's claims does not exclude any given row or column of vias to be the desired claimed structure. Therefore, the references as detailed above have been modified to remain outstanding rejections of the claimed invention.

The insertion of Applicant's additional claimed language, for example, "in claims 1 and 8" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Field of Search	Date
U.S. Class and subclass: 257/758,700,701,774-776,786,784,680,207-211,797	3/22/03 9/19/03
Other Documentation: foreign patents and literature in 257/758,700,701,774-776,786,784,680,207-211,797	3/23/03 9/19/03
Electronic data base(s): U.S. Patents EAST	3/23/03 9/19/03

Papers related to this application may be submitted to Technology Center 2800 by facsimile transmission. Papers should be faxed to Technology Center 2800 via the Technology Center 2800 Fax center located in Crystal Plaza 4-5B15. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center 2800 Fax Center number is (703) 308-7722 or 24. Only Papers related to Technology Center 2800 APPLICATIONS SHOULD BE FAXED to the GROUP 2800 FAX CENTER.

Any inquiry concerning this communication or any earlier communication from the examiner should be directed to ***Examiner Alexander Williams*** whose telephone number is **(703) 308-4863**.

Any inquiry of a general nature or relating to the status of this application should be directed to the ***Technology Center 2800 receptionist*** whose telephone number is **(703) 308-0956**.

9/20/03

Primary Examiner
Alexander O. Williams